Karlsruher Institut für Technologie

Examination SS 2013

Communication Systems and Protocols

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Communication Systems and Protocols
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Prerequisites for the examination

Aids

- Allowed aids for the examination are writing utensils, a ruler, a non-programmable calculator and a single sheet of A4 paper with self- and hand-written notes. Writing may be on a single side of the paper only. The use of own concept paper is not allowed.
- Use only indelible ink - use of pencils and red ink is prohibited.
- Other aids than that mentioned above is strictly forbidden. This includes any type of communication to other people.

Duration of the examination

120 minutes

Examination documents

The examination comprises 30 pages (including title page). Answers may be given in English or German. A mix of language within a single (sub)-task is not allowed. In your solution mark clearly which part of the task you are solving. Do not write on the backside of the solution sheets. If additional paper is needed ask the examination supervisor. It may not be possible to finish all tasks within the duration of the examination. This will be accounted for within the grading of the exam.
You will not be allowed to hand in your examination and leave the lecture hall in the last 30 minutes of the examination.
At the end of the examination: Stay at your seat and put all sheets into the envelope. Only sheets in the envelope will be corrected. We will collect the examination.

		Page	*~ Pts [%]*	*Points*
Task 1	Error Protection	2	17%	18
Task 2	Media Access	6	14%	16
Task 3	Synchronization	11	13%	15
Task 4	Data Transmission	15	8%	10
Task 5	Physics	17	15%	17
Task 6	Practical Aspects of Communication Systems	21	15%	17
Task 7	Networks	26	18%	20
				Σ 112

Task 1 Error Protection 18

Task 1.1 Error Detection

A) Name two methods for error detection within a communication protocol based on redundancy. 1

Parity Check, Block Check, XOR Block Check, Hamming Code

B) To which extend can Parity Checking be used to detect burst errors? Justify your answer. 1

Parity checking can detect all burst errors with an odd number of errors

Task 1.2 CRC-Calculation

The bitstream 10110011 shall be coded and transmitted using the generator polynomial $g(x)=x^6+x^5+x^3+x^2+1$.

A) Give the bitstring for the given generator polynomial 1

Bitstring for generator polynomial: 1101101
Point is also given if bitstring is given correct in B) or C)

B) Determine the bitstream as it is being transmitted. 4

Bitstring for generator polynomial: 1101101

Degree of generator polynomial = 6, hence six zeros need to be appended

```
10110011000000 : 1101101
1101101
01101001
 1101101
 00001000000
     1101101
     01011010
      1101101
      01101110
       1101101
       0000011        Remainder: 000011
```

Bit stream as it is transmitted: 10110011000011

1pt: bitstream appended with six 0's
2pts: calculation correct (remainder = 0)
0pts if systematic error
1pt if single calculation error
0pt more than 1 calc error
1pt: correct bitstream that is being transmitted

C) With a transmission system that uses CRC for error protection, a sender transmits the following bitstream: 10110011000011. **3**

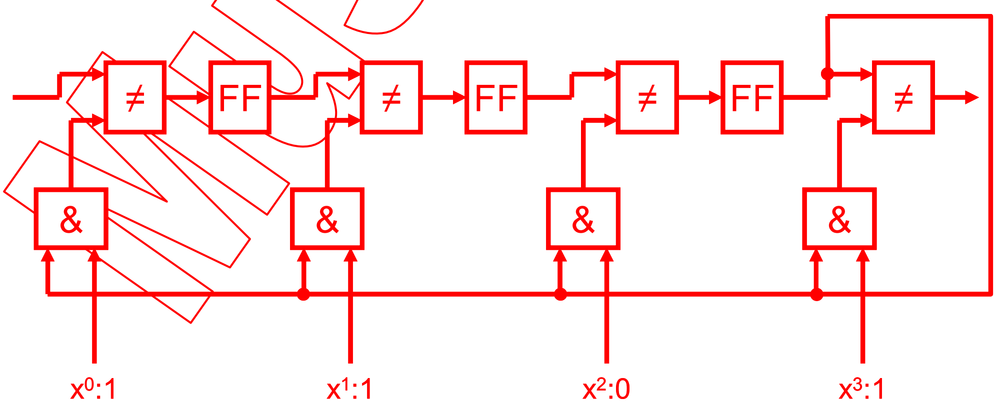
Carry out the CRC error detection scheme of the receiver, assuming that the generator polynomial $g(x) = x^6+x^5+x^3+x^2+1$ has been used. What does the receiver conclude from the result?

```
10110011000011 : 1101101
1101101
01101001
 1101101
 00001000000
     1101101
     01011011
      1101101
      01101101
       1101101
       0000000
```

The remainder of the division is 0 therefore the receiver will assume that the transmission is error free.

2pts:	***calculation correct (remainder = 0)***
	0pts if systematic error
	1pt if single calculation error
	0pt more than 1 calc error
1pt:	***receiver ASSUMES an error free transmission***

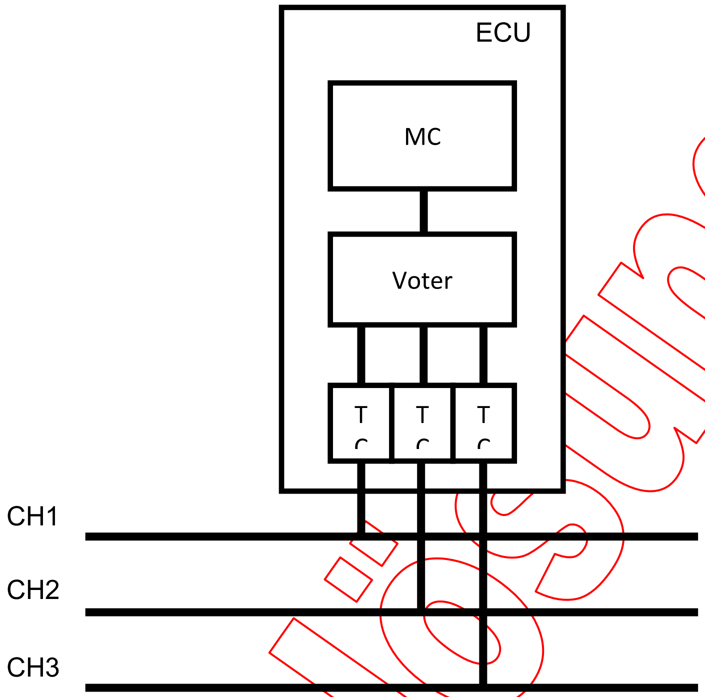
D) Given is the bitstring 1011 of a generator polynomial. Draw the full (not the simplified) hardware realization of the decoder by means of flip flops, XOR and AND gates. **3**



1pt: correct main elements used, consisting of AND+XOR+FF
1pt: correct AND inputs (x0, x1, x2, x3)
1pt: feedback from FF to all AND gates

Task 1.3 External Redundancy

The figure below illustrates a setup of a bus system using multiple parallel channels (CH1, CH2, CH3). Data that is received by an electronic control unit (ECU) is read off the bus via transceivers (TC). Subsequently it passes a voter before it is processed within a microcontroller (MC).



A) What is the task of the voter? 1

Decides about correct/corrupted transmission by comparison of incoming data from different redundant channels.

B) Assume the following: 2
1) Only a single error is possible at any point in time in the whole system
2) Errors are only injected over bus lines
3) Only external redundancy is used for error detection.
Question: What is the minimal number of redundant channels necessary in order to be able to detect transmission errors? Justify your answer.

Two redundant channels are necessary. The voter compares data on both channels. If data differs, there must be an error, although it is not possible to say which channel has an error.

1pt: correct number
1pt: justification

C) Assume the same preconditions as in B). How many redundant channels are necessary in order to be able to correct transmission errors? Justify your answer.

2

Three redundant channels are necessary. If all three channels deliver the same value, either all three are working properly (most likely) or all three have failed in same manner (most unlikely). If two have the same value, most likely the channel that differs has failed and we can rely on the value data delivered by the two identical channels -> Hence correction is possible.

1pt: correct number
1pt: justification

Task 2 Media Access

16

Task 2.1 Multiple use of media

A) For transmitting data of multiple nodes at the same time different access schemes exist. Name two access schemes other than CDMA.

1

CDMA = Code Division Multiple Access

FDMA = Frequency Division Multiple Access

TDMA = Time Division Multiple Access

SDMA = Space Division Multiple Access

0.5 points per scheme

B) Give the Walsh-functions for the transmission of four nodes at the same time.

1

Function 1	+1	+1	+1	+1
Function 2	+1	-1	+1	-1
Function 3	+1	+1	-1	-1
Function 4	+1	-1	-1	+1

Table 2.1: Walsh-functions

Point only given for correct table
CAREFUL: Order can be different

Also correct substitution:
+1 = 0
-1 = 1
Or vice versa

For a CDMA access scheme the first three chips of the Walsh-functions from the subtask above got lost. Sending the bits listed in table 2.2 the signal **0 4 0 0** can be measured on the medium.

	Walsh-function				**send bit**
A	+1	-1	+1	**-1**	**1**
B	+1	+1	+1	**+1**	**0**
C	+1	+1	-1	**-1**	**0**
D	+1	-1	-1	**+1**	**1**

Table 2.2: CDMA scheme using Walsh-functions

C) Complete table 2.2 with the correct missing chips. Justify your answer by giving all your calculation steps or your complete reasoning.

4

+1	+1	+1	+1	
0	4	0	0	
0	+4	0	0	0 was send

Last bit of Walsh is +1 and 0 was send, therefore has to be node B

+1	-1	+1	-1	
0	4	0	0	
0	-4	0	0	1 was send

Last bit of Walsh is -1 and 1 was send, therefore has to be node A

+1	+1	-1	-1	
0	4	0	0	
0	+4	0	0	0 was send

Last bit of Walsh is -1 and 0 was send, therefore has to be node C

+1	-1	-1	+1	
0	4	0	0	
0	-4	0	0	1 was send

Last bit of Walsh is +1 and 1 was send, therefore has to be node D

1pt: correct function assignment

Points when using calculations:
2pts: for correct calculations of correlation)
1 pt: interpreting the sum correctly correct

Points when using reasoning:
3pts for correct reasoning
1pt for ansatz (2nd chip is resulting in +4)
1pt for ansatz (inverting functions)
1pt for assigning 1 and 0 (deciding what function is inverted)

2nd solution:

The sum of the second chips has to be +4. Therefore function 2 and 4 must be inverted. Assuming that sending '1' means inversion of the Walsh function, function 2 and 4 can be assigned to function B or C (or vice versa). Because the last chip of function 2 is -1 it has to be assigned to function B.

D) What are the general advantages and disadvantages of CDMA? (list one advantage and one disadvantage) **1**

0.5 points for each correct answer

Pro:

More robust against narrowband disturbances because signal energy is distributed on a broader spectrum

Lower sensitivity against interferences from other nodes

Better protection against eavesdropping As the signal looks like white noise, it is impossible to detect when a transmission is going on

Eavesdropper has to know the used pseudo random sequence in order to be able to reconstruct the send data

Contra:

More effort required an sender and receiver side

Requires channel with larger bandwidth

Task 2.2 Arbitration

A) For the arbitration of four nodes a Tap-line model is used. Draw a Tap-line model with four nodes. Label all used signals. Give a short explanation (one sentence) of each of the different types of signals used in this scheme. Mark the arbiter in your scheme and briefly explain its basic function (ca. 3 sentences). **3**

Request: If node wants to send, it signalize it with dominant level on Request line

Grant: gives access of transmission line to one exclusive node

0.5 points for each explanation

Node signalizes his request on the request line. The arbiter gives grant to one exclusive node, regarding the priority initialized in the arbiter.

1 point for correct description

A system using centralized daisy-chaining is shown in figure 2.1. An exemplary arbitration cycle of the system is shown in figure 2.2.

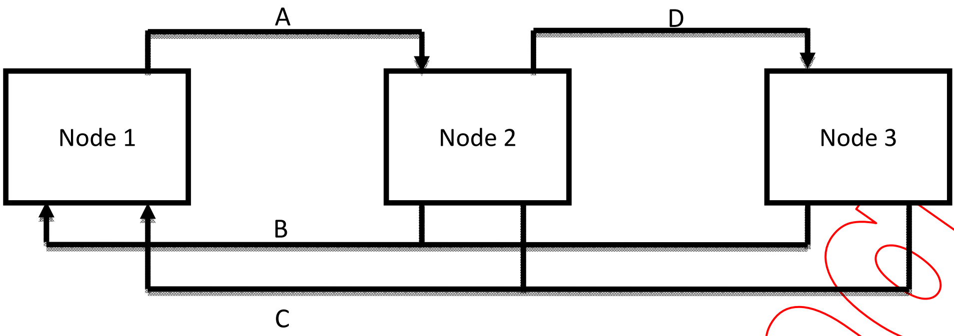


Figure 2.1: Centralized Daisy-chain

B) Assign the correct signals of figure 2.1 to the signals shown in the diagram below (figure 2.2). Justify your choice of assignment with a few sentences.
What node is sending data at which point in time? Complete the diagram (figure 2.2) accordingly. 3

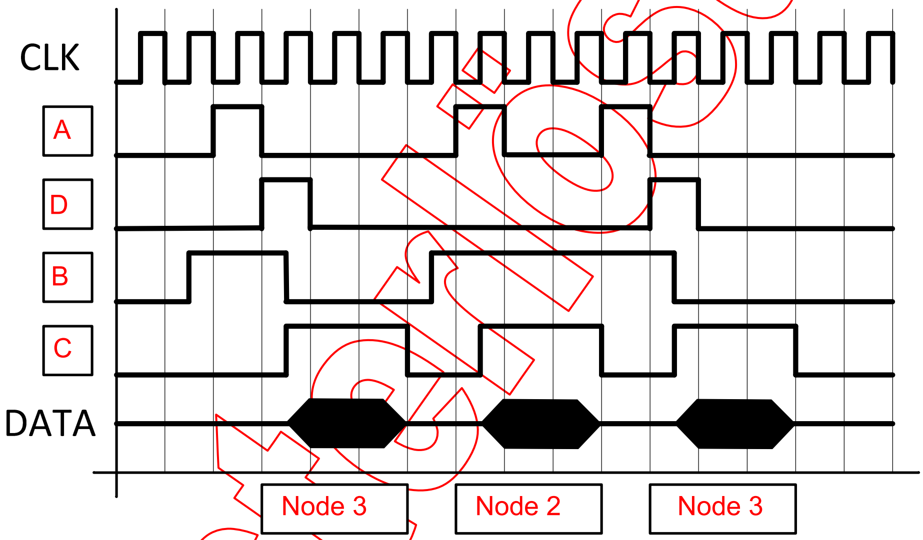


Figure 2.2: Signal flow for Daisy-chain

If C and B are exchanged it has to be exchanged at explanation as well.

Lowest signal has to be C/B because it is the busy line, which is high while data is transmitted.

Second to last signal has to be B/C, because it is a request line which triggers the token/grant and gets low while sending.

A and D are both grant or token signals.

First has to be A, because it is a token/grant and it starts first.

Second has to be D, because it is a grant and it always starts after A.

2 Points for left labels

+0.5 points for each correct description and label in Figure 2.2

1 Point for correct sending nodes

+0.5 points if only two are right

In the decentralized Daisy-chain shown in figure 2.3 a scheduling should be done. The different nodes will set a request at the times given in table 2.3. Only after successful transmission the nodes will remove their request. The sending of the data always needs exactly one time step. This includes token passing and the time needed for the arbitration.

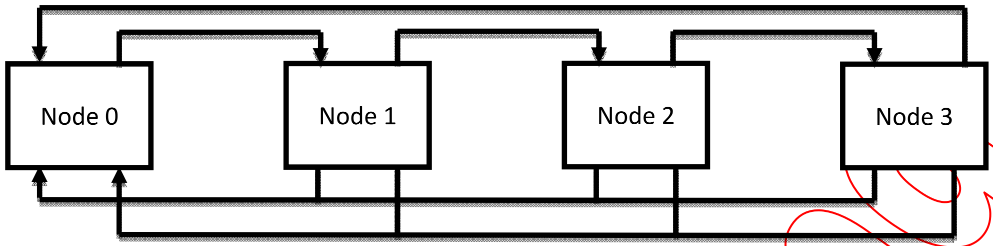


Figure 2.3: Decentralized Daisy-chain

time	Nodes that assert a sending request signal
t_1	Node 2 and Node 3
t_2	Node 1
t_3	Node 0
t_4	Node 0 and Node 1

Table 2.3: Time of sending nodes

C) Complete Table 2.4 according to the specified arbitration scheme. **3**

0.5 points for each row of table

time	Sending node
t_0	Node 0
t_1	Node 2
t_2	Node 3
t_3	Node 0
t_4	Node 1
t_5	Node 0
t_6	Node 1

Table 2.4: Solution of Daisy-chain scheduling

Task 3 Synchronization

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Task 3.1 Synchronization methods

A) Characterize the synchronization methods in the table below with respect to the given transmission types.

3

Transmission methods	Parallel	Serial	Synchronous	Asynchronous
Shared/dedicated clock line	x		x	
Start-stop mode		x		x
Suitable line code		x	x	
Handshake mode	x			x
Scrambler		x	x	

-0.5P for each false/missing X

min. 0P

B) Using the table below, compare the given methods with respect to the synchronization characteristics/properties and cost. Only one example per cell is necessary.

3

Method	Advantages	Disadvantage
Dedicated clock line	• Easy to determine the bit intervals • No data signal modification needed	• More signal line => expensive • Parallel transmission => skew
Suitable line code	• Less signal lines => less cost • Timing recovery	• higher bandwidth needed => expensive
Scrambler	• Less signal lines => less cost • Timing recovery	• Additional logics needed for inserting and extracting scrambler bits => expensive

+0.5P for each correct box

Task 3.2 Hand-shaking partners

A communication system is given in **Fehler! Verweisquelle konnte nicht gefunden werden.**. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a half-duplex hand-shake protocol corresponding to Figure 3.1 for the high-level synchronization.

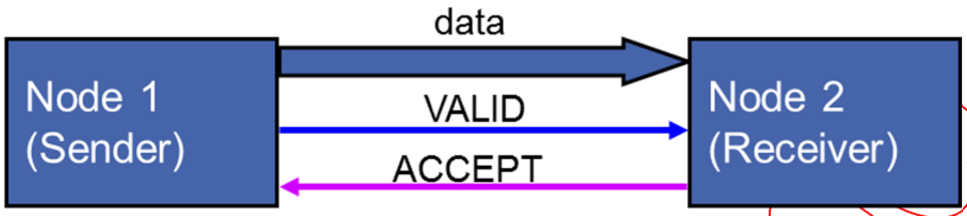


Figure 3.1: Communication system applying half-duplex hand-shake procedure

A) In Figure 3.2, the sensitive clock edges of the sender and the receiver as well as the signals' values for the first sender's clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the *valid* signal is set to '1' by the sender. The receiver will also set the *accept* signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale. 4

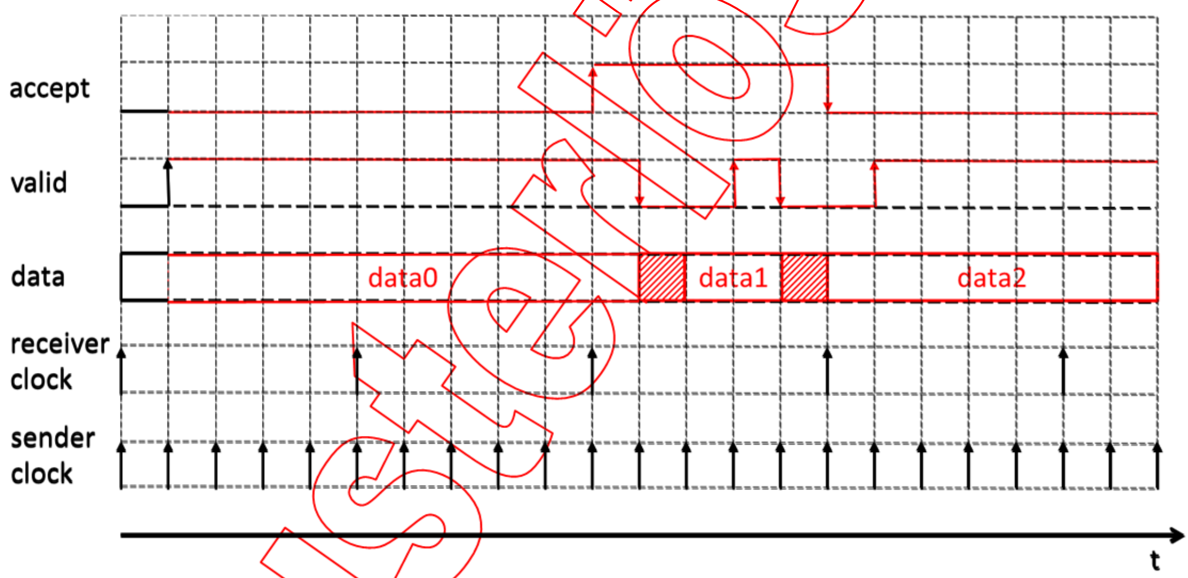


Figure 3.2: Signal progression diagram

Correct idea of "accepted" half-duplex hand-shaking *+2P*
(data => valid=1 => accept=1 => valid=0 => data => valid=1 etc.)
Each wrong/missing step *-0.5P*

Timing behavior is completely correct *+2P*
Each timing error *-0.5P*
(data1 may directly follow data0; the same for data2 and data1)

B) Is this kind of synchronization free from error in this specific case? Justify your answer. **1**

No. One can see that data1 got lost because it was put on to the data lines and removed by sender while receiver is still busy processing data0.

Recognize that data1 is lost	***+0.5P***
Correct reasoning for the data lost	***+0.5P***

C) Propose a better solution for this communication scenario. **1**

1. Clock divider in sender so that both are only clocked at 200 kHz.
2. Apply a full-duplex hand-shaking protocol.
3. Clock down the sender: to avoid this loss of data, the following equation must be satisfied:

$$3Tr \leq 2Tr + 4Ts$$

$$\Rightarrow \quad Tr \leq 4Ts$$

The receiver's clock frequency of must be more than or equal to one-fourth of the sender's one.

1pt: One correct solution

Task 3.3 Against noise with tied hands

3

You are to design a data communication system with a data rate of 25 Mbps. However, the given communication channel is noisy. Statistics shows that during one bit interval, one noise pulse, which causes the signal to be misinterpreted (bit flipping), may occur with a maximum duration of 15 ns. Due to resource constraints, neither are you allowed to switch to another channel, nor is it possible to modify the sender, which does not integrate any mechanism for error correction. What can you do in order to make your system works correctly (statistically seen)? Rationalize your solution.

Oversampling with minimum factor k (due to resource constraints) is needed => k samples available.
Data rate r = 25 Mbps => Bit interval l = 1 / (25x10^6) = 40 ns

If k=1 => the only sample point may be overlapped => bit flipping may occur.
If k=2 => distance between sample points is d = 40/2 = 20 ns, noise pulses may only overlap 1 of them. However, there is no way to distinguish which sample point holds the right value.
If k=3 => d = 13,3 ns, noise pulses may overlap 2 of 3 sample points => bit flipping may occur.
If k=4 => d = 10 ns, noise pulses may overlap 2 of 4 sample points => same situation as if k=2
If k=5 => d = 8 ns, noise pulses may overlap max. 2 of 5 sample points => the bit can be recognized correctly using majority voting.

Result: oversampling with factor 5 is needed.

Alternative solution: low-pass filter!

Correct method: oversampling	***+0.5P***
Minimal value of k needed	***+0.5P***
Correct bit interval	***+0.5P***
Correct value of k	***+0.5P***
Reasoning for value of k	***+1P***

10

Task 4 Data Transmission

Task 4.1 Transmission Rate

The CSMA/CD media access control as used in Ethernet includes a collision detection method. Thereby, a sender transmits a jam signal if it detects another signal while transmitting a frame. The jam signal must propagate to all receivers before the transmission ends. This introduces a minimum frame size for Ethernet that is coupled to the maximum wire length. The minimum frame transmission time must be higher than the time required passing a maximum length wire twice.

A) Calculate the minimum frame size in bytes of an Ethernet network running at 100 Mbit/s over a coaxial cable with the following parameters? 2

2 pts: correct result
Else 1pt: correct Ansatz

Transmission rate: 100 Mbit/s

Maximum cable length: 500 m

Propagation speed of coaxial cable: 200000 km/s

Minimum frame transmission time: 1 km / 200000 km/s = 1 / 2 * 10^5 = 5 * 10^-6 s

Minimum frame size: 5*10^-6 s * 1*10^8 Bits/s = 500 Bits

= ⌈500/8⌉ Byte = 62,5 Byte

➔ When sending full bytes: 63 Byte

B) Calculate the minimum efficiency of the transmission system when sending only dataframes with minimum frame size and an overhead of 100 bits per frame are required. 1

(500 – 100 bits) / 500 bits = 80%

1 pts: correct result
0,5pts: 500/(500+100)=83,333…

C) The maximum frame size for ethernet is 1500 bytes. Would you use CSMA/CD together with 10 Gbit Ethernet? Please explain your answer. 2

No, the minimum frame size for 10 Gbit Ethernet is 50,000 bits and this is larger than the maximum frame size.

1 pt: correct answer
1 pt: explanation

Task 4.2 Shannon Limit

A) What is the Shannon Limit? **1**

The Shannon Limit tells the maximum rate at which information can be transmitted over a communications channel of a specified bandwidth in the presence of noise.

1 pt: correct answer

B) Calculate the Shannon Limit for a channel with 1000 Hz bandwidth and a S/N of 127. Give the result in bits/second. **1**

CS = fmax·* log2(1+S/N) = 1000 Hz·* log2(128) bit = 7000 bit/s = 7 kbit/s

1 pt: everything correct

C) Calculate the required signal-to-noise ratio (SNR) in dB for a channel with 1 MHz bandwidth and a transfer rate of 3 Mbit/s. **3**

CS = fmax·* log2(1+S/N)

- ⇨ Log2(1+S/N) = CS / fmax
- ⇨ S/N = 2^ (CS / fmax) - 1
- ⇨ S/N = 2 ^ (3 Mbit/s / 1 Mhz) -1 = 2^3 - 1 = 7
- ⇨ SNR = 10 log(7) = 8,95 dB

1 pt: Ansatz (take formula and reorder it to S/N)
1 pt: dB conversion (method)
0.5 pts: calculation of S/N correct
0.5 pts: dB conversion correct

Task 5 Physics

17

Task 5.1 General questions

A) What are parameters of a periodic signal? Name 2 parameters.

1

Period T or Frequency 1/T

Amplitude S(t)

Phase φ

0.5 pt per parameter (1 pt max)

B) Several modulation techniques were discussed in the lecture. Name 3 of them and describe shortly their functionality.

3

Amplitude Modulation, Amplitude Shift Keying

Linear change in amplitude in radio broadcasting.

Frequency Modulation, Frequency Shift Keying

Linear change in frequency in radio broadcasting.

Phase Modulation, Phase Shift Keying

Phase jumps in digital systems.

Quadrature Amplitude Modulation

Combination of ASK and PSK.

Pulse Modulation

Varying a digital signal to represent an analog value.

1 pt for naming and description of 1 modulation technique
0.5 pt for naming of 1 modulation technique

C) What does cut off frequency mean?

1

This is the frequency at which the signal amplitude has dropped by 3 dB compared to the output value.

1 pt for correct answer
0.5 pt not possible

Task 5.2 DA/AD-Conversion

A) What is the minimum frequency an analog signal has to be sampled with in order to allow perfect reconstruction of the analog signal? Give the equation and the name of the theorem.

1

$$f_{sample} \geq 2 * f_{max}$$

Nyquist-Shannon-Sampling Theorem

1 pt for correct theorem and equation

B) Why and when is a sample & hold element necessary?

1

The sample & hold element holds the analog signal constant during the AD conversion.

1 pt for correct answer
0.5 pt not possible

C) Oversampling: Explain what oversampling means and name the advantages.

1

Digital oversampling:

N sample points per bit (n-times oversampling)

Majority voting among the samples → value that appears most is taken

Advantage: Filtering of short distortions is possible

Analog oversampling:

Multiple sampling of the signal

Sampling steps has to be in the specified range.

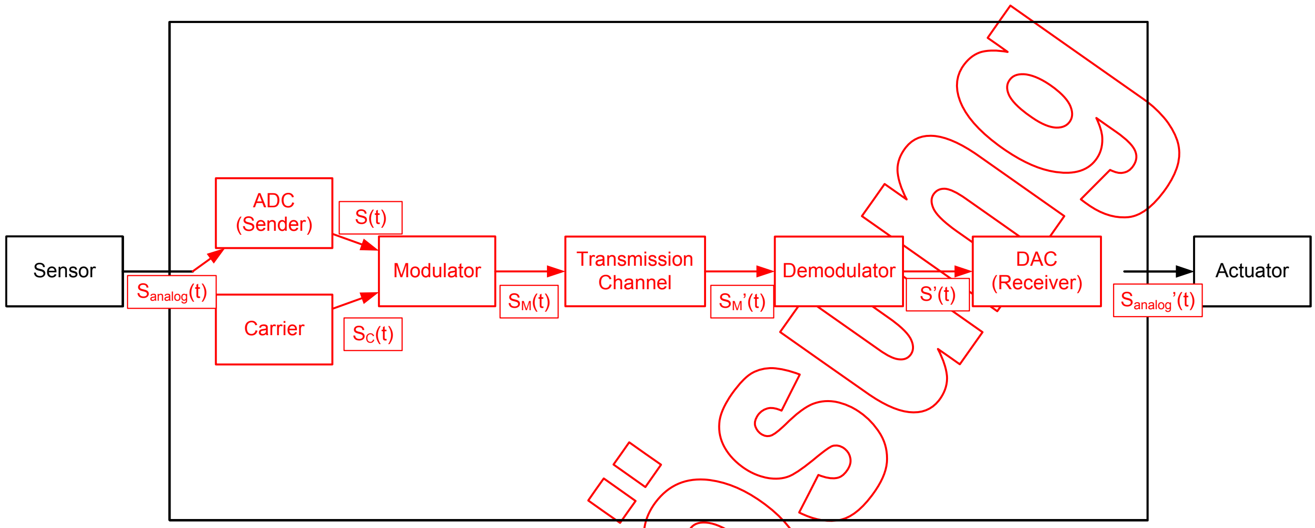
Advantage: Compensation of failures

1 pt explained digital or analog oversampling with advantages
0.5 pt for advantage or explained oversampling

Task 5.3 Modulation

4

An analog signal is send from a sensor to an analog actuator. It has to be modulated with frequency shift keying. Draw in a block diagram the complete transmission chain of the signal and name all necessary blocks with their corresponding signals. Give a short description of the task of each block and signal.



Sender: delivers the source signal S(t) which has to be send.

Carrier: carrier signal which is given to the modulator $S_C(t)$

Modulator: carrier signal is added to the source signal, so the carrier is modulated.

Transmission channel: the modulated signal is send over the transmission channel

Demodulator: receives the modulated signal $S_M(t)$ more or less distorted. A good approximation of the modulated signal is filtered by the demodulator s'(t)

Receiver: receives the demodulated signal s'(t)

1 pt for sender and receiver with correct description and signals
1 pt for carrier with correct description and signals
1 pt for modulator and demodulator with correct description and signals
1 pt for transmission channel with correct description and signals

Only 1 pt if the block diagram is drawn correct without description

Task 5.4 Reflection on wires

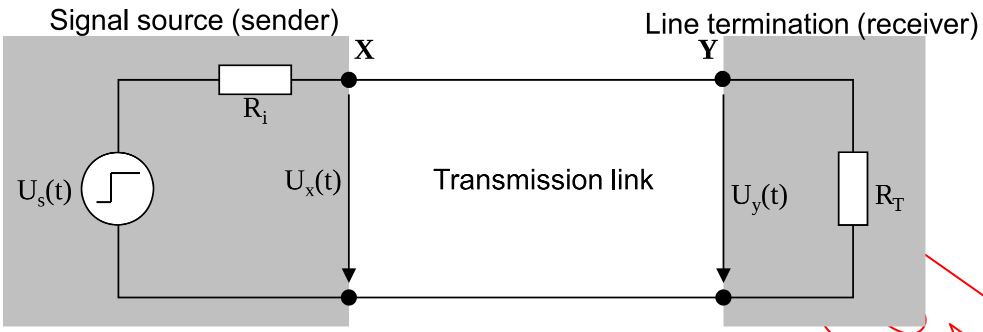


Figure 5.1: Test Setup

A) In Figure 5.1 an assembly is considered, consisting of a voltage source with an internal resistance R_i = 75Ω as sender and a receiver with R_T = 250Ω. The DC resistance of the line is zero. Calculate the value of the wave resistance at the time of t=0. **2**

At the time t=0 the voltage U_s of the sender changes from 0V to 6V and is constant afterwards. The runtime of a wave on the wire is t_d. The voltage u_x at the time of t=0 is $U_x(0)$ = 4V.

$$u_x(0) = u_s \cdot \frac{Z_w}{R_i + Z_w}$$

$$Z_w = \frac{\frac{u_x(0)}{u_s} R_i}{1 - \frac{u_x(0)}{u_s}} = \frac{\frac{4V}{6V} 75\Omega}{1 - \frac{4V}{6V}} = 150\Omega$$

1 pt for correct equation
1 pt for correct result

B) Calculate the reflection factor on receiver side of the test setup in **Fehler! Verweisquelle konnte nicht gefunden werden.**. **1**

$$r = \frac{R_T - Z_w}{R_T + Z_w} = \frac{250\Omega - 150\Omega}{250\Omega + 150\Omega} = 0{,}25$$

1 pt for correct equation and result
0.5 pt for correct equation

C) Which value has the reflection factor on receiver side if the termination resistance is ∞? **1**

$$r = 1$$

1 pt for correct result
0.5 pt not possible

D) When does a perfect wire adaption exist? **1**

r = 0, $R_T = Z_w$.

1 pt for correct answer

Task 6 Practical Aspects of Communication Systems

17

Task 6.1 General Questions

A) Which factors are constraining the throughput of parallel busses? Name 2 factors.

1

Bus width
Skew (routing)
Clock frequency (critical path, parasitics, fanout, input capacitances, …)
Attenuation

B) What is the difference between synchronous and asynchronous communication?

1

In **synchronous communication** a **clock** signal is transmitted along with the data. No synchronization logic is needed in the receiver.
In **asynchronous communication** there is **no dedicated clock** signal. The received data needs to be synchronized and in case of variable baud rate, a clock recovery needs to be done on the receiver side.

C) How many layers does the TCP/IP internet reference model have?

four

1

D) Explain the difference between a LAN switch and a router.

A **LAN switch** is setting up point-to-point connections (no broadcast compared to HUBs) **between the participants in a local area network**.
A **router** is routing network packets **among several networks**.

1

Router works on Level 3 and switches on Level1 or Level 2.

Task 6.2 Serial Protocol

In Figure 6 a serial protocol is given.

PREAMBLE	START	ADDR	EXP	CMD	BCNT	STATUS	DATA	CHK

Preamble: 5 bytes 0xFF (settling time)

Start character: 1 byte

Address: source and destination, 1 byte

Expansion field: 1 byte

Command: 1 byte

Byte count: 1 byte (≥0x02)

Status: 2 byte

Data: (BCNT-2) bytes

Checksum: 1 byte

Figure 6: Serial protocol with 9 fields

A) Is the total length of a message fixed or variable? Please justify your answer and specify the total length if it is fixed or the minimum and maximum length of the packet if it is of variant size **2**

The length of the message is variable, because the length of the data field is variable and is specified by the BCNT field. The range of the length of the message is between (5+1+1+1+1+1+2+0+1)=13 and (5+1+1+1+1+1+2+253+1)=266 bytes.

1 pt for variable length (only with justification)
0,5 pt minimum value
0,5 pt maximum value

B) Which field(s) is/are indicating that the protocol from Figure 3 is used for an asynchronous communication? How could a resynchronization work here? **2**

Preamble and Start. The preamble 0xFF causes a defined stable 'high' value on the line for the duration of 5 bytes and allows the signal to settle. A following well defined start field marks the cycle accurate beginning of a message after the settling period.

1 pt for Preamble and/or start
1pt for description

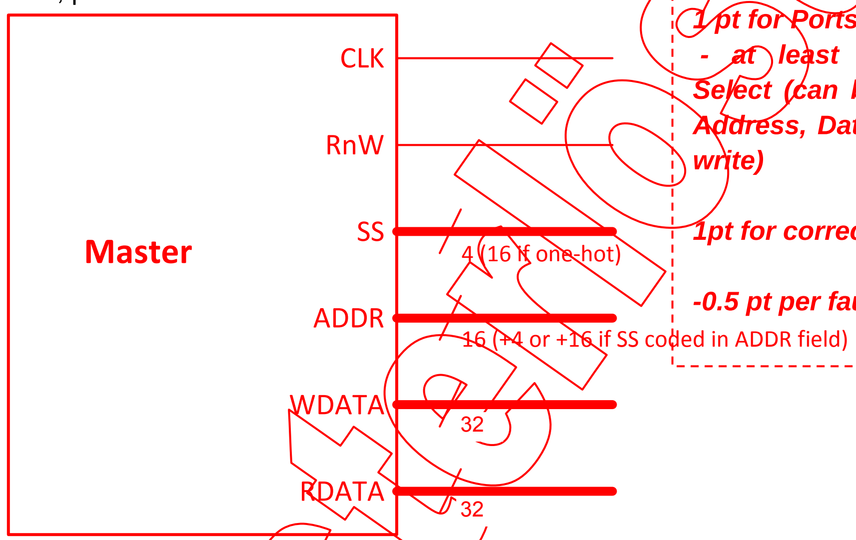
Task 6.3 Development of a custom bus

For a specialized system-on-chip a synchronous on-chip bus for communication between a master module and several slave modules needs to be developed.

The requirements are:

- Clock synchronous
- Parallel bus
- No tri-state drivers
- Separate bus lines for read data and write data
- Width of data busses is 32 bit
- Address range from 0x0000 to 0xFFFF in each slave
- Maximum 16 slave modules possible

A) Please draw a "black box" of the master module, containing all necessary ports. In case of bus lines, please mark the bus widths. **2**



1 pt for Ports:

- at least CLK, Read/Write, Slave Select (can be also in Address field), Address, Data (separate for read and write)

1pt for correct signal width

-0.5 pt per fault

B) Is there a difference in the slave modules concerning the signals or the widths? Justify your answer? **1**

Yes, the slave module needs only one select signal…

or (in case SS is integrated in ADDR field):
Yes, the address width is smaller since only the bit indicating the respective slave is needed…

or
No, the slave select is decoded inside the slave module…

Task 6.4 Timing diagram of asynchronous bus

In Figure 7 an asynchronous parallel bus for interfacing e.g. NOR Flash memories is given. A description of the interface signals is given in Table 4.

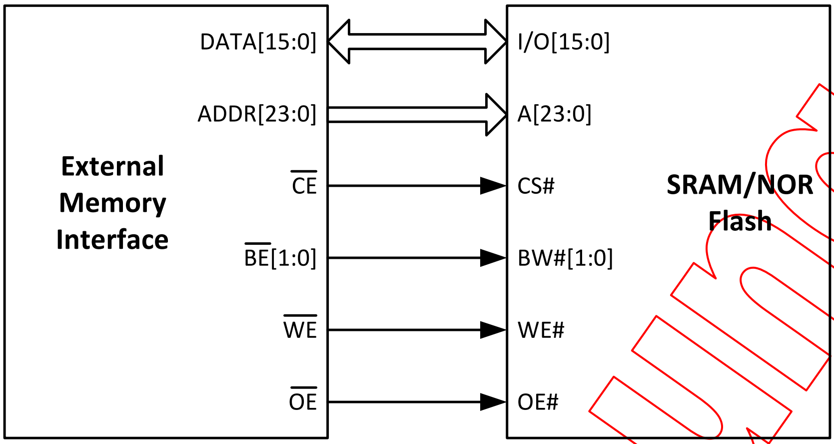


Figure 7: External memory interface with asynchronous bus, connected to a Flash memory

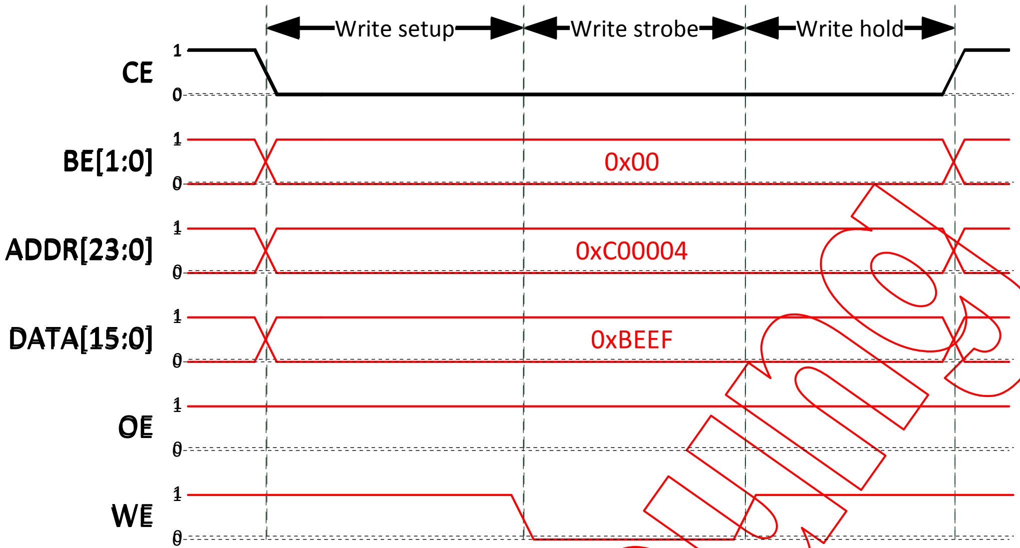
Table 4: Description of the interface signals

Port	Description
DATA [15:0]	Data I/O pins. 16/8-bit bidirectional data path for I/O.
ADDR [23:0]	External address outputs.
CE[3:0]	Chip select for CE space. Active-low chip select for memory spaces 0 to 3.
BE[1:0]	Active-low byte enables (Upper and lower). Individual bytes or half-words can be selected: “00” = data on DATA[15:0], “01” = data on DATA[15:8], “10” = data on DATA[7:0]
OE	Active-low output enable. Low during read access period.
WE	Active-low write enable. Low during write transfer strobe period.

Since the bus is asynchronous, read and write accesses are taking place in three phases:

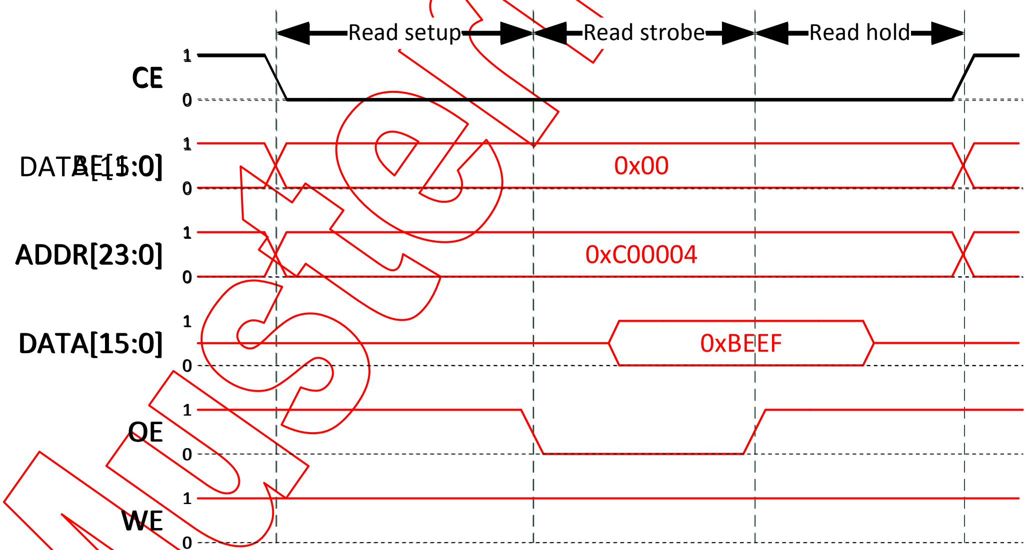
1. **Setup:** Phase between the beginning of a memory cycle (chip select low, address valid, byte enable valid, write data valid) and the activation of read or write strobe.
2. **Strobe:** Phase between the activation and deactivation of the read (OE) or write (WE) strobe.
3. **Hold:** Phase between the deactivation of the read or write strobe and the end of the cycle (which may be either an address change or the deactivation of the chip select signal.

A) Please complete the signal changes in the timing diagram below for a write access of data 0xBEEF at address 0xC00004! Consider the above named phases! **3**



1 pt: BE, ADDR and DATA stable during phases
1pt: only Strobe active in second phase
1pt: Correct value of OE, WE

B) Please complete the signal changes in the timing diagram below for a read access at address 0xC00004! Consider the above named phases! **3**



Task 7 Networks

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Task 7.1 XY-Routing

Figure 7.1 shows a 4x4 meshed Network-on-Chip with bidirectional links for packet based communication.

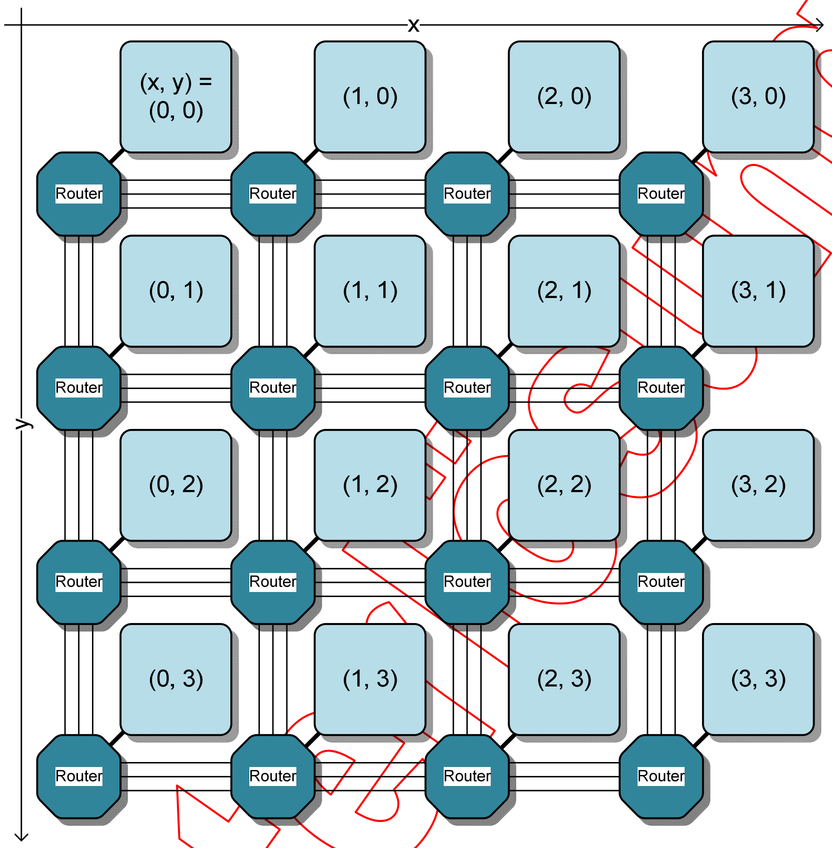


Figure 7.1: 4x4 meshed Network-on-Chip

For the following it is assumed, that XY-routing is used.

A) Which routers are passed by a packet sent from (x, y) = (1, 1) to (2, 3). Please provide the coordinates of the passed router in the order given by the transmission process. 1

(1, 1), (2, 1), (2, 2), (2, 3)

+ 0.5 Pt. per 2 node

Now, there is an error on the NoC, blocking the link between router (1, 1) and (0, 1).

B) Is router (3, 1) affected by this error? If so, which are the destination nodes to which router (3, 1) cannot communicate anymore (give the coordinates)? **1**

(0, 0), (0, 1), (0, 2), (0, 3)

+ 0.5 Pt. per 2 node

C) XY-Routing enables deadlock-freedom by avoiding turns. Which turns are these? **1**

South-West, South-East, North-West, North-East

Turns from column into a row are prohibited

180° turns

1pt: correct explanation or complete list of correct turns

D) Comparing centralized and distributed routing: Give one advantage for each strategy **2**

Centralized Routing: global optimization possible,

reduced complexity in each router

Distributed Routing: scalability due to no communication overhead,

Fast reaction on changing routing requirements

+ 1 Pt. per valid advantage

E) Besides centralized and distributed routing there exist other routing methods. Give two of them. **1**

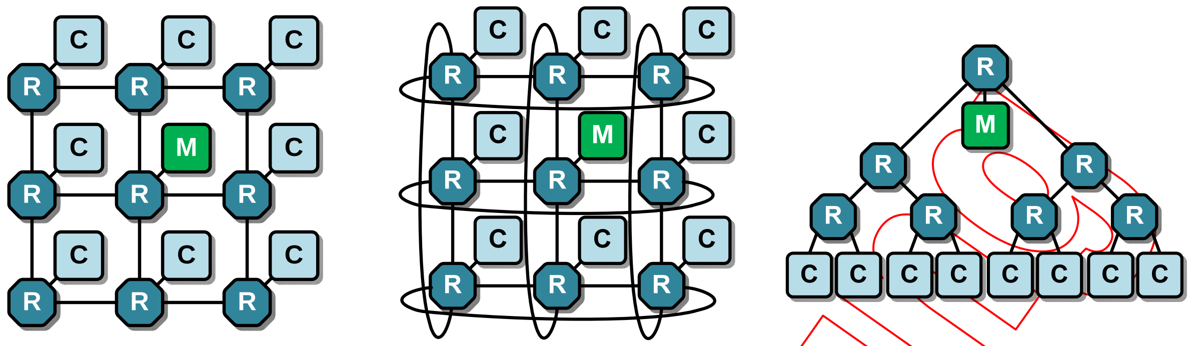
Source Routing, Static Routing, Adaptive/Dynamic Routing,

Unicast Routing, Multicast Routing, Broadcast (e.g. Flooding)

+ 0.5 Pt. per routing method

Task 7.2 Topologies

In the following three different topologies: (a) Mesh, (b) Torus and (c) Binary Tree will be investigated under different constraints. All links can be assumed to be bi-directional.



(a) Mesh (b) Torus (c) Binary Tree

Select the best suitable topology and reason your choice:

A) Fair access of all nodes to a shared memory: 2

A binary tree where the shared memory node is located at the root of the tree

+ 1 Pt. per correct topology
+ 1 Pt. per valid reason

B) Lowest number of hops taken on average for data transmission: 2

The number of direct neighbors of a node within a topology is a measure for the average communication distance / hop count. Torus has the highest number of neighbors and thus the lowest average hop count.

+ 1 Pt. per correct topology
+ 1 Pt. per valid reason

C) Highest number of link error tolerable before inaccessibility of one node: 2

A torus NoC can tolerate at least up to 3 link errors,
A mesh can tolerate at least 1 link error and a binary tree cannot tolerate any errors. Thus, torus is best.

+ 1 Pt. per correct topology
+ 1 Pt. per valid reason

Task 7.3 Circuit- and Packet-Switching

In the following different requirements are given. Please select the switching method that fits best to the given requirement. 3

Requirement	Circuits-Switching	Packet-Switching
Low latency (transmission of 1 byte of data, no connections established)		X
Low latency (transmission of 1 byte of data, connections established)	X	
Real time guarantees	X	
Energy Consumption	X	
Flexibility		X
Short and non-frequent data transfers		X

+ 0.5 Pt. if correct

Task 7.4 OSI Reference Model

Figure 7.2 shows the 7 layers and the layer names of the OSI reference model

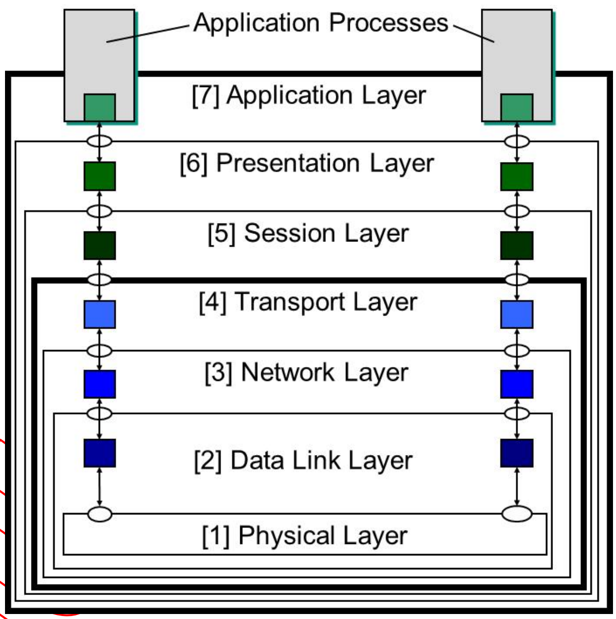


Figure 7.2: The seven layers of the OSI reference model

A) Please give the highest layer of the ISO model shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**, that is used by the following components: 2

Router: **[3] Network Layer / ([4] Transport Layer)**

Hub: **[1] Physical Layer**

Repeater: **[1] Physical Layer**

Bridge: **[2] Data Link Layer**

+ 0.5 Pt. per device layer

The following latencies for data processing within each layer of the OSI reference model can be assumed for all devices in the following:

[1] Physical Layer:	0.1 us
[2] Data Link Layer:	10 us
[3] Network Layer:	100 us
[4] Transport Layer:	0.5 ms
[5] Session Layer:	1 ms
[6] Presentation Layer:	1.5 ms
[7] Application Layer:	2.5 ms

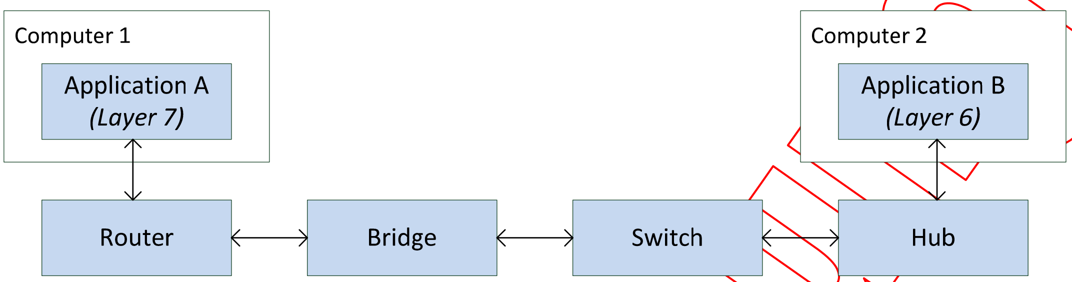


Figure 7.3: Data transmission scenario

In Figure 7.3 the communication between Application A and Application B is shown. The payload size can be assumed as small. Thus, data transmission latency is assumed to be independent from the payload size. Links between devices are short and transmission delay can be assumed to be zero. Communciation between devices is done on the physical layer.

B) Please calculate the communication latency of each device on the communication path between Application A and Application B shown in Figure 7.3. **3**

Computer 1:

Layer[7] + Layer[6] + Layer[5] + Layer[4] + Layer[3] + Layer[2] + Layer[1] = 5,6101 ms

Router:

2 * Layer[3] + 2 * Layer[2] + 2 * Layer[1] = 220,2 us

Bridge:

2 * Layer[2] + 2 * Layer[1] = 20,2 us

Switch:

2 * Layer[2] + 2 * Layer[1] = 20,2 us

+ 0.5 Pt. per device latency

Hub:

2 * Layer[1] = 0.2 us

Computer 2:

Layer[6] + Layer[5] + Layer[4] + Layer[3] + Layer[2] + Layer[1] = 3,1101 ms